REMARKS

Claims 1-12 and 14 are pending in the application. Claims 1, 2, 4, 6-8, and 11 have been amended hereby. Claims 1, 4, 6, 7, 8, and 11 are in independent form. Favorable reconsideration is requested.

The title of the invention has been changed to read --HIGHLY INTEGRATED MULTIPROCESSOR SYSTEM--. Withdrawal of the objection to the specification is requested.

Claim 2 has been amended to correct the informality pointed to in the Office Action in paragraph 2. Withdrawal of the objection to the claim is requested.

Reconsideration is respectfully requested of the rejection of Claims 1-12 and 14 under 35 U.S.C. §103(a), as being obvious over U.S. Patent No. 6,807,620 ("Suzuoki") in view of U.S. Patent No. 5,706,478 ("Dye") and U.S. Patent No. 6,671,196 ("Cilvin").

The present invention relates to a multiprocessor system including at least a first processor and a second processor. The first processor includes an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction in a running main routine, the interrupt being for requesting to store a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction. The second processor includes an address save unit which saves the return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction to a predetermined memory area when the second processor receives an interrupt from the interrupt generation unit, as recited in amended independent Claim 1. See paragraph [0027] of the filed application, for example.

Salient features of the presently claimed invention are that the main processor performs some processes which were originally performed by the graphic processor. Specifically, the

main processor performs, for the graphic processor, storing a return address and extracting an address that is set in a plurality of commands dividedly when the graphic processor executes a call or a jump instruction, and transferring a return address if a return instruction for retuning to the calling source is executed in a subroutine. Because of these features, even a graphic processor that has simple hardware resources can process multiple stages of call instructions. It is respectfully submitted that the cited references, alone or in any possible combination, if any, fail to teach or suggest the aforementioned features of the presently claimed invention.

Dye, as best understood, discloses a technique where a host CPU makes a coprocessor such as a graphic processor execute commands of a display list. Dye focuses on how the host CPU packetizes some commands that the graphic processor executes. Although a call instruction, etc. are described in the specification of Dye, such instructions are a part of the command requested by the host CPU, and a return address is stored in a stack in a graphic processor. Therefore, the host CPU does not perform either storing a return address, extracting a destination address, nor notifies the return address for the graphic processor, which are a part of the process for executing a call instruction, a jump instruction, etc. Further, the interrupted signal generated by the graphic processor in Dye is for notifying the completion of the commands, not for requesting to perform a part of the process for the call instruction, as in the presently claimed invention. See col. 16 line 66 to col. 17 line 4 of Dye, for example.

Cilvin, as best understood, discloses a technique where the data stored in a register is moved to a stack cash according to a progress in a program for later restoring so that the frequency of the access to the primary memory can be decreased. In this technique, when the stack cash becomes full, the data is moved to the primary memory. However, the technique of Cilvin does not include a process where one processor delegates the task to store or restore return

address to another processor, as in the presently claimed invention. The description of col. 5 lines 22-40 in Cilvin, cited for these features, does not correspond to the interrupt generation unit of the presently claimed invention, because the process in Cilvin is quite different from an "interrupt," which is typically transmitted from one device to another.

Regarding Claim 4, in Cilvin, cited for these features, there is no description of an address extraction unit which extracts a call destination address or jump destination address stored dividedly in formats of the call instruction or the jump instructions and an accompanying execution stop instruction.

Amended independent Claims 6, 7, 8, and 11 recite features similar in many respects to the features of discussed above with respect to amended independent Claims 1 and 4.

Accordingly, it is respectfully submitted that amended independent Claims 1, 4, 6-8, and 11, and the claims depending therefrom, are patentably distinct over the cited references, alone or in any possible combination, if any.

In view of the amendments and remarks set forth above, this application is believed to be in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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